AMENDMENTS

In the Specification:

Please amend the paragraph starting on page 14, line 13, as follows:

In this regard, each bit of an m-bit decoded register identifier corresponds to a particular general register 29. When a decoder 84 receives an n-bit register identifier that identifies one of the general registers 29, the decoder 84 is configured to assert the bit in the m-bit register identifier that corresponds to the one general register 29 and to deassert the remaining bits in the m-bit register identifier. Therefore, by detecting which bit in the m-bit decoded register identifier is asserted, it can be determined which general register 29 is identified by the m-bit decoded register identifier. Commonly assigned U.S. Patent Application entitled "System and Method for Efficiently Detecting Data Hazards Between Instructions of a Computer Program," ~~(atty. docket no. 10971185)~~ assigned serial no. 09/490,390, and filed on January 24, 2000, and commonly assigned U.S. Patent Application entitled "System and Method for Utilizing Instruction Attributes and Register Identifiers to Detect Data Hazards Between Pipeline Processed Instructions," ~~(atty. docket no. 10971333)~~ assigned serial no. 09/490,389, and filed on January 24, 2000, which are both incorporated herein by reference, describe in more detail circuitry that may be used to implement the decoders 84 and circuitry that may be used by hazard detection circuitry 81 to detect when the register identifiers of two instructions match and, therefore, when a data hazard may exist between the two instructions.